Analysis of the Cost of Embedded Passives in Printed Circuit Boards

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Abstract
This paper summarizes an application-specific economic analysis of the conversion of discrete passive resistors and capacitors to passives that are embedded within a printed circuit board, i.e., integral substrates. In this study we assume that embedded resistors are printed or plated directly onto wiring layers (as opposed to requiring a dedicated layer), that bypass capacitors are embedded by dielectric substitution into existing reference plane layers, and that singulated non-bypass capacitors are embedded using dedicated layer pair addition. The model performs three basic analyses: 1) Board size analysis is used to determine board sizes, layer counts, and the number of boards that can be fabricated on a panel; 2) Panel fabrication cost modeling including a cost of ownership model is used to determine the impact of throughput changes associated with fabricating integral substrates; and 3) Assembly modeling is used to determine the cost of assembling all discrete components, and their associated inspection and rework. The combination of these three analyses has been used to evaluate size/cost tradeoffs for an example boards.

Introduction
The use of discrete passive components in electronic systems has continued to increase even as the degree of system integration has increased. To meet the increased demand for passive devices some passive devices are fabricated within ICs, however, designing passives into ICs limits the IC's flexibility for many uses. In addition, real estate on an IC is usually more expensive than real estate on a board.

The increased demand for passives not only requires more passives to be purchased and assembled to the system, but also suggests that discrete passives will consume increasing amounts of board area and assembly time. The electronics assembly industry has responded to the challenge by developing higher-speed chip shooters, and the passive components industry has responded by producing smaller passive components.

An alternative solution to the passive growth trend is integrating multiple passives together within a single package (networks or arrays of passives). This approach can reduce assembly costs, however, the unit cost of integrated passives remains high (generally higher than the discrete passive components they replace). Even with the use of small dimension passives and judicious insertion of network or array passive components, many applications still cannot meet performance and size requirements. Embedded passives (fabricated within integral substrates) were introduced to address these needs. Embedded passives are fabricated within substrates, and while embedded passives will never replace all passive components, they provide a potential advantage for many applications including:

- Increased circuit density
- Decreased product weight
- Improved electrical properties,

and possibly…

- Cost reduction
- Increased product quality
- Improved reliability.

Potentially the biggest single question about embedded passives is their cost, "…of all the inhibitors to achieving an acceptable market for integral substrates, the demonstration of cost savings is paramount".[1] There is considerable controversy in technology circles as to whether applications fabricated using embedded passives will be able to compete economically with discrete passive technology. On the positive side, the use of embedded passives reduces assembly costs, shrinks the required board size, and negates the cost of purchasing and handling discrete passive components. However, these economic advantages must be traded off against the increased cost (per unit area) of boards fabricated with embedded passives (a situation that will not disappear over time), lower yield of layer pairs containing embedded passives, and decreased throughput during board fabrication.

In this paper we present a model for assessing the application-specific economics of converting discrete passives to embedded passives. The next section outlines the model formulation followed by sample results generated using the model.

Model Formulation
The objective of the model discussed in this paper is to capture the economic impact of the following

competing effects when embedded components are present in the board:

- Decreased board area due to a reduction in the number of discrete passive components
- Decreased wiring density requirements due to embedding passives
- Increased wiring density requirements due to the decreased size of the board
- Increased number of boards fabricated on a panel due to decreased board size
- Increased board cost per unit area
- Decreased board yield
- Decreased board fabrication throughput
- Decreased assembly costs
- Increased overall assembly yield
- Decreased assembly-level rework.

Due to the opposing nature of many of the effects listed above, the overall economic impact of replacing discrete passives with embedded passives is not trivial to determine and, in general, results in application-specific guidelines instead of general rules of thumb. In fact the very nature of tradeoff analysis is one in which *the greater the detail necessary to accurately model a system, the less general and more application-specific the result.*

Several authors,[1-7] have addressed cost analysis for embedded passives and thus provide varying degrees of insight into the economic impact of converting discrete passives to embedded. The target of all these economic analyses is to determine the effective cost of converting selected discrete passive components to embedded components. The most common approach to economic analysis of embedded passives is to: 1) reduce the system cost by the purchase price and conversion costs (handling, storage and assembly) associated with the replaced discrete passives, 2) reduce the board size by the sum of the layout areas associated with the replaced discrete passives and determine the new number of boards on the panel, and 3) determine the new board cost based on a higher per unit area cost for the integral passive panel fabrication and the new number-up computed in step 2. The results of these three steps determine the new system cost. The effects included in this first-order approach are critical, however, the approach generally ignores several additional elements, most notably: possible decreases in throughput for integral substrate fabrication mean that board fabricators will have to charge higher profit margins on integral substrate to justify their production on lines that could otherwise be producing conventional boards; routing analysis of the board to determine not only what layers may be omitted, but what layers may have to be added to maintain sufficient wiring capacity as passives are embedded and the board is allowed to shrink; yield of both discrete passive components and the variation in board yield due to the embedding of passives; and potential reductions in rework costs (due to both assembly defects and intrinsic functional defects) associated with discrete passives.

In the model presented here, we incorporate quantitative routing estimation and assess board fabrication throughput impacts for setting profit margins on board fabrication, effects that have not been included previously.

The model used for analyzing embedded passives is outlined in Figure 1. The detailed formulations used in the model are documented elsewhere,[8] qualitatively the model works in the following way:

1) Accumulate the area of footprints of discrete passives to be embedded. Determine the area occupied by each plated or printed embedded resistor on wiring layers.
2) Reduce board area by accumulated discrete passive area from 1) maintaining the aspect ratio of the original board. This step is optional, i.e., the board area may be fixed.
3) Plated or Printed Resistors: Perform routing analysis removing nets and vias associated with resistors that are embedded and accounting for area blocked by embedded resistors on wiring layers. Routing is assumed to be unaffected by discrete resistors embedded using Ohmega-Ply® or similar approaches. Bypass Capacitors: All nets and vias associated with embedded bypass capacitors are removed from the routing problem. Singulated Capacitors: Assume embedded singulated capacitors do not affect routing analysis. Using these assumptions determine the relative change in routing resources due to embedding selected passives.
4) Using the layer requirements, the relative routing requirements for the integral substrate and either a fixed measure of the routing efficiency associated with the conventional board or a range of possible efficiencies determined under the assumption that the conventional version of the board did not include any more layer pairs than it needed to route the problem, compute the number of required layer pairs for the embedded passive implementation.
5) Determine the yield of layer pairs that include embedded passives.
6) Determine the trimming cost for embedded resistors. The necessity of trimming is determined by the resistor's tolerance. The application-specific cost per trim is determined by modeling the throughput of a laser trimming process.[9]

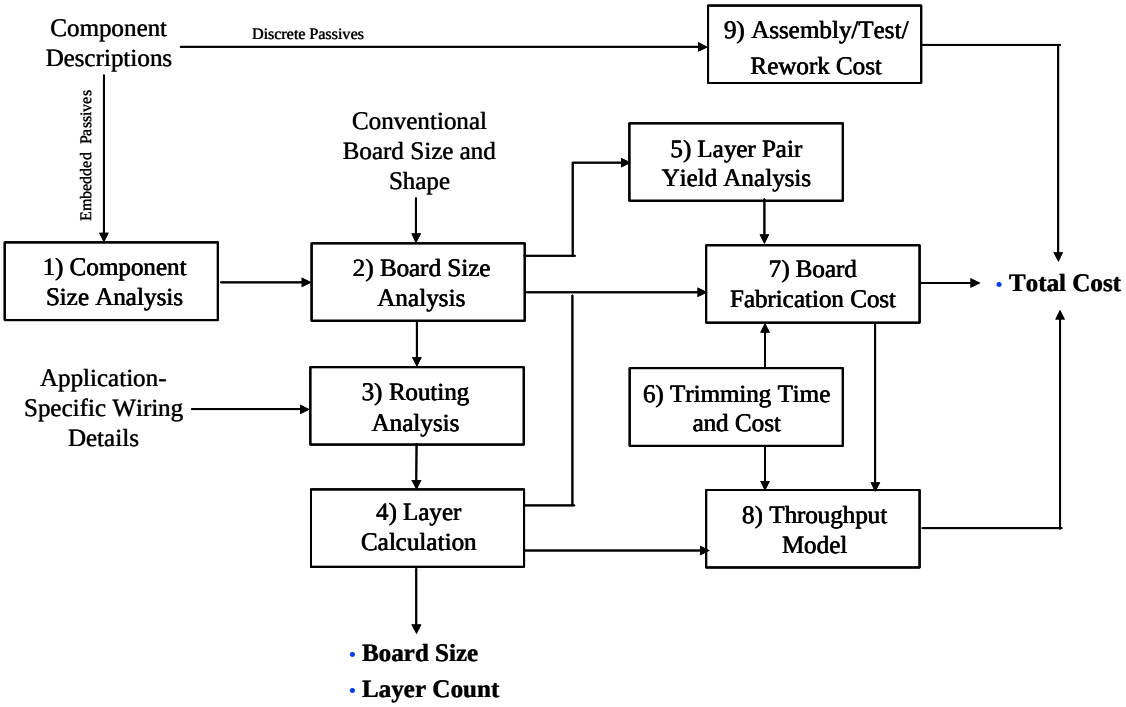

Figure 1 – Summary of cost model developed for the analysis of embedded passive cost impacts on electronic systems.

7) Compute the number of boards per panel from the board size (number-up) and the effective panel fabrication costs from the layer and material requirements, yields, and resistor trimming costs.
8) Determine the relative board fabrication profit margin from layer pair throughput modeling (see discussion later in this section).
9) Accumulate assembly cost, test, rework, and board fabrication (with profit margin) to obtain total relative cost.

The model generates two system costs, one with no discrete passives embedded and one with a mix of discrete and embedded passives (the specific mix is user defined). Because the analysis ignores all non-embeddable parts, all functional testing of the system, and other cost elements that are approximately equivalent for the embedded and conventional system, the significant result is the difference in system cost between these two solutions.

The following technology assumptions are made:

1) Embedded resistors fabricated directly on wiring layers via printing or plating are supported,[10] in addition to approaches that require dedicated embedded resistor layers.
2) Bypass capacitors are embedded by dielectric substitution into an existing reference plane layer (as opposed to layer pair addition).
3) Singulated embedded capacitors are fabricated via dedicated layer pair addition.

Throughput Modeling[8] - One fundamental issue not addressed in previous cost analyses associated with embedded passives is the throughput of the process that is used to manufacture the layer pairs. Throughput is key to understanding the profit margin that will be required to justify integral substrates.

A situation that the board manufacturer may face is the following: assume that there are two types of boards that could be fabricated on a process line, one is a conventional board and the other is an integral substrate. The manufacturer must decide what profit margin to use for the integral substrate so that the total profit per unit time made by selling integral substrates equals or exceeds what can be made by selling the conventional boards. This may be necessary to justify the use of a line to fabricate integral substrates when it would otherwise be producing conventional boards. So, not only is it more expensive (materials, labor, tooling, equipment) to produce integral substrates, but, if fewer can be produced per unit time, the manufacturer will likely need to charge a higher profit margin in order to realize an equivalent profit per unit time.

Implementation - The model described herein has been implemented in a web-based analysis tool, Figures 2 and 3.

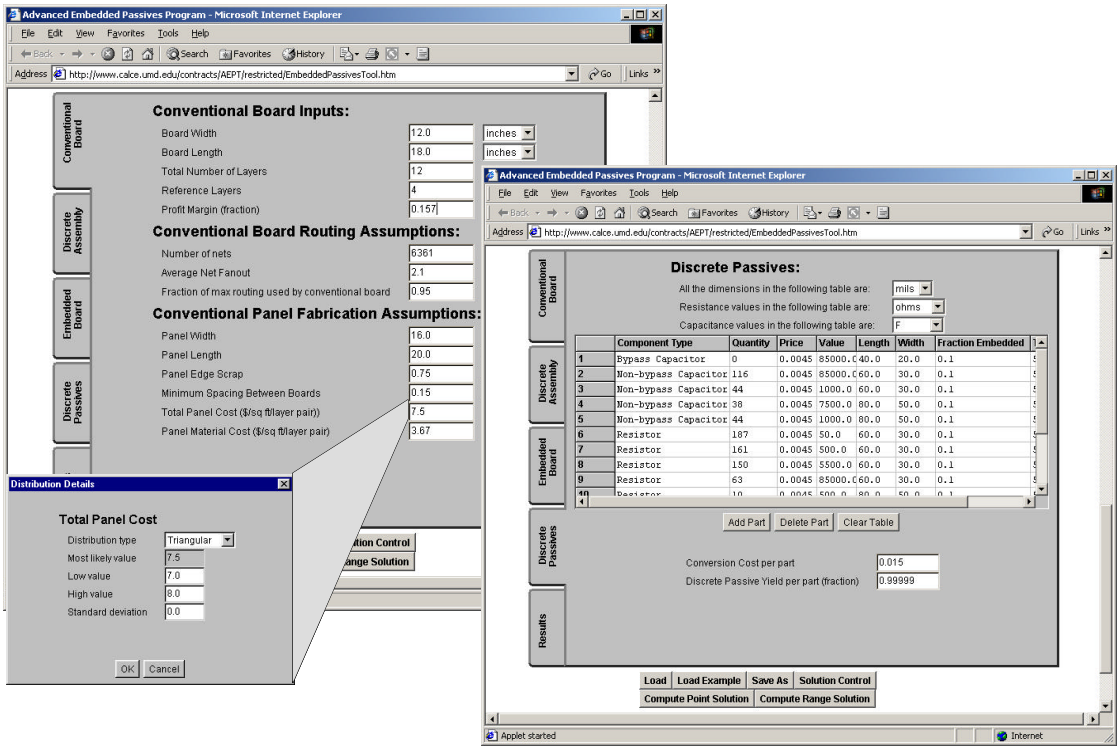

Figure 2 – Embedded passive cost modeling tool interface examples. The dialog box in the lower left corner collects inputs in the form of probability distributions for Monte Carlo analysis.

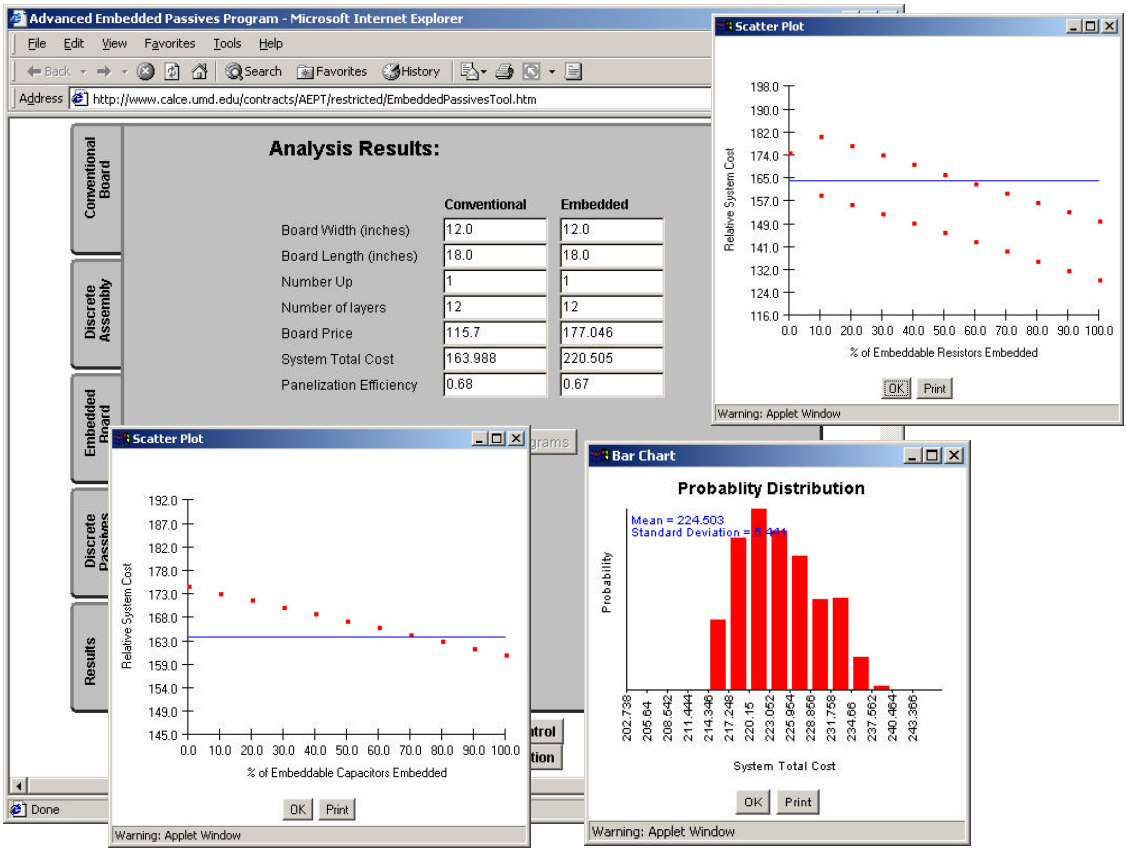

Figure 3 – Embedded passive cost modeling tool results and output examples.

To accommodate uncertainties in input data, the model has been implemented within a Monte Carlo analysis framework. Each non-integer input can have a designated distribution type. Random numbers are used to select values from the distributions with which to perform the analysis. When a sufficiently large sample size has been completed, histograms of the output parameters can be created and mean and standard deviations of the solutions determined.

Example Results

In this section we present the results of size/cost tradeoff analyses performed on a fiber channel card. It is not the intent of this analysis to prove that embedded passives lead to less expensive systems, rather we wish to understand the economic realities should we decide to use embedded passives.

The fiber channel card application has 610 embeddable resistors and 242 embeddable bypass capacitors. Figure 3 shows analysis results for the fiber channel card as discrete resistors are replaced by embedded resistors (no capacitors are embedded in Figure 3). Relative system cost is plotted in Figure 3 indicating the system cost less the cost of all non-embeddable components and functional testing. The fiber channel board's conventional implementation is on a 12 x 18 inch board, two possible panel sizes are considered. The solution bands in Figure 3 indicate that for both panel sizes, economical solutions that include embedded resistors (plated) are possible. The data points when no resistors are embedded (0%) represent the board price increase due only to the need for a higher profit margin to justify integral substrate fabrication. The next point (larger) on the vertical axis is the relative cost of the system when the first resistor is embedded.

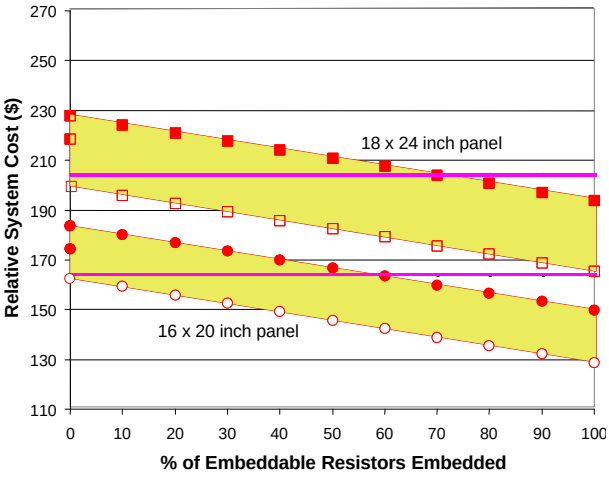

Figure 3 - The economics of embedded resistors (plated on wiring layers) for the fiber channel card application. The data points represent one embedded passive solution for a specific routing resource assumption[8] (assumption of the ratio of resources actually used to route the conventional implementation of the board and the theoretical maximum amount of resources that could be used), the band represents all possible integral passive solutions for this application; the solid horizontal line is the system cost of the conventional implementation.

The results for embedding the bypass capacitors in the fiber channel board are shown along with the results for two other applications in Figure 4. The economics of embedded bypass capacitors can be generalized by observing the application-specific embeddable bypass capacitor density necessary to breakeven on system costs, i.e., by plotting the embeddable bypass capacitor densities where the cost difference between the conventional and embedded passive implementations is zero,

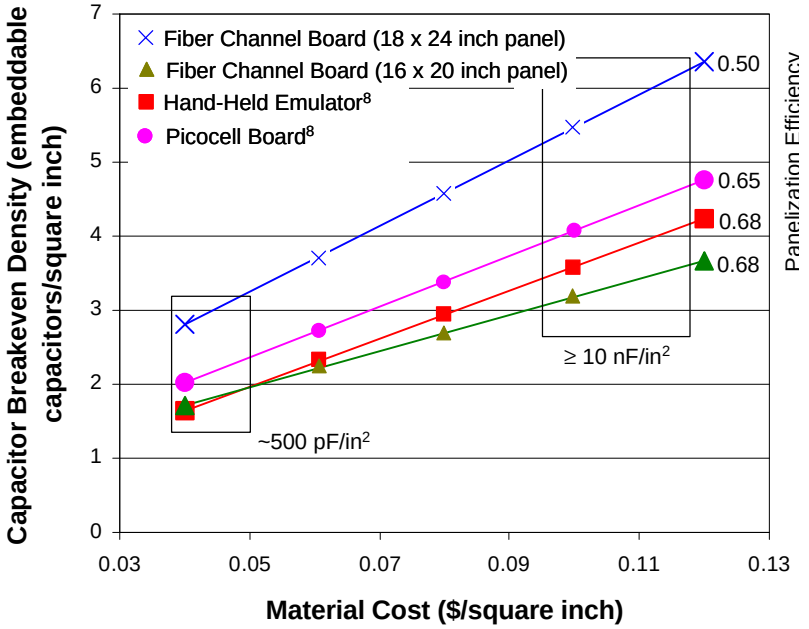

Figure 4 - Bypass capacitor breakeven densities as a function of dielectric material replacement costs. Only single layer substitution is considered in this plot. The actual capacitor densities: Fiber Channel Board – 1.12 caps/in^2, Picocell Board – 2.76 caps/in^2, Hand Held Emulator – 23.44 caps/in^2.

Figure 4 shows the general result for three applications. The critical assumptions for this plot are: the board size and the number of layers required for routing is not allowed to change. The primary differentiator between the applications, as far as this plot is concerned, is the panelization efficiency (the total board area on the panel divided by the panel area). The dielectrics used to produce embedded capacitor layers are relatively expensive and would be purchased and used at the panel size, therefore, a low panelization efficiency indicates that the application is wasting a lot of the expensive material, versus a larger panelization efficiency indicates less waste and therefore lower breakeven capacitor densities are possible.

Discussion and Conclusions

In this paper we have presented an application-specific economic analysis of the conversion of discrete passive components (resistors and capacitors) to passives that are embedded within a printed circuit board. The model has been demonstrated on a fiber channel card. In this case and others documented elsewhere,[8] we found embedded resistors (plated or printed onto existing wiring layers as opposed to dedicated embedded resistor layers) to be generally cost effective with the most significant economic impact resulting from either number-up increases due to board size reductions, or layer count decreases due to reductions in routing requirements. Note, we do not generalize embedded resistor economics to some critical components per unit area measure because it is board fabrication profit margin driven, which is a fractional increase in board cost and much smaller in absolute terms for high number-up, whereas cost reduction is through omission of discrete part costs. As expected, when a technology that adds resistors directly to the wiring layers is used, embedded resistors become economically viable when considerably fewer are embedded than for layer addition technologies.

Bypass capacitor embedding economics is tied to panelization efficiency and the cost of the dielectric material. In general, it is more difficult to make sound arguments for embedded bypass capacitors based solely on economics than for embedded resistors. From Figure 4 and the actual bypass capacitor densities in its caption, it can be seen that the hand-held emulator can be economically produced using embedded bypass capacitors (due to its large actual bypass capacitor density), but in order to gain an economic advantage for the fiber channel card one must be able to replace all the bypass capacitors using a single layer pair (with dielectric material costing less than $0.05/sq inch) and implement it on a 16x20 inch panel. The picocell board on the other hand is economical if a single layer of $0.085/sq inch dielectric material can be used.

It must be reiterated that due to the opposing nature of many of the effects listed outlined in this paper, the overall economic impact of replacing discrete passives with embedded passives, in general, yields application-specific guidelines instead of general rules of thumb. We also need to point out several system implementation details are not addressed in this analysis including:

i. Waste disposition in board fabrication – we only account for additional waste disposition costs associated with the fabrication of integral substrates in the profit margin differential.
ii. Non-homogeneous panelization – some panel fabrication technologies and materials allow boards to be laid out on the panel with 90 degree relative rotations resulting in the potential for more boards on a panel, we have assumed homogeneous panelization in this analysis.
iii. We have not considered the possibility raised previously[1] that the conversion of discrete to embedded passives may allow some double-sided assemblies to become single sided thus saving significant assembly costs.
iv. In addition to the direct effects on system cost discussed in this paper, there are many other "life cycle" effects on the system cost. These effects include the changes in the system reliability, performance, end-of-life options and the design overhead that constitute effective life cycle costs. For some systems, embedded passives may also affect the upgradability and field repairability of the system.

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