Yield Learning Simulation

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Abstract

In this paper, a method to predict defect-related yield as a function of time for a semiconductor manufacturing facility is presented. The effect of contamination-related defects on yield, and the reduction in defect levels, resulting from failure analysis, have been considered. The developed yield learning model is incorporated in a prototype simulator ,Y4 ,which mimics both the fabrication and the failure analysis processes. Results are presented for a spectrum of examples to illustrate the use of the simulator, in formulating IC manufacturing strategies.

Introduction

In any semiconductor design/manufacturing operation important strategy decisions are made whenever new product is planned and then developed. These decisions have a direct impact on the success of the product measured in terms of profit and/or an ability to maintain a competitive edge. For volume production, these measures can be directly translated to the notion of *time-to-market* and *time-to-money*. A short time-to-market and time-to-money can be achieved if manufacturing yield is acceptably high right from the beginning of the production cycle or when yield ramps up very quickly [1]. In reality, however, neither of the above is easily achieved. This is because of the complex nature of the relationship between the attributes of the fabricated ICs, the factors responsible for yield loss and organization of the manufacturing and failure analysis processes. Objective of this paper is to propose yield simulation techniques which models the above relationship in order to aid design/manufacturing strategy making process.

In the paper, we have focussed on simulation techniques which captures the change of yield with time, for a multi-product fabrication line. We have concentrated on contamination-related defects causing functional failures in the IC. We also assumed that the failure analysis facility is aimed at these defects and modifying the fabrication line reducing defect levels. We have shown subsequently that the results of our simulation can reveal certain useful properties of the manufacturing process which cannot be analyzed otherwise.

This paper is organized as follows. In the next section, we have presented modeling techniques for predicting change in yield with time. The next section describes the implementation of the prototype simulator. A spectrum of sample experiments are presented next, followed by conclusions.

Yield Learning Model

A new yield modeling philosophy postulated in this paper is based on the following rationale. A manufacturing process can be viewed as consisting of two phases: manufacturing phase and failure analysis phase, as shown in Figure 1. In the fabrication phase, wafers are processed in a sequence of steps defined by the process recipe. At each step, a unique piece of equipment is used, and specific layer is defined. In this phase, each equipment introduces manufacturing defects leading to functional yield loss. In the second phase, failure analysis is performed on a fraction of the fabricated wafers to determine the cause of the failure. Based on this analysis, corrective actions are taken on the piece of equipment supposedly responsible for the observed defects.

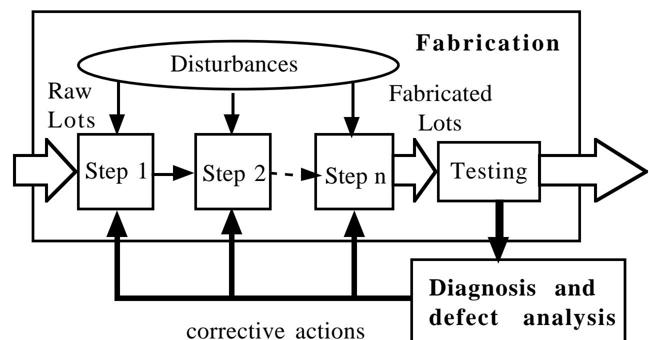

Figure 1. Manufacturing process to be modeled.

Hence, in order to model the yield learning process one should be able to model manufacturing and failure analysis processes as a sequence of events. The focus should be on process and design attributes which affect timing and efficiency of activities causing decrease of defect levels.

In other words the key elements of yield learning model must be the computations of:

a. Level of contamination introduced by each manufacturing step.
b. Probabilities of correct diagnosis by failure analysis.
c. Timing of manufacturing and failure analysis events.

The above observations lead to the development of a simulation method using an event based model to time the fabrication and failure analysis processes. Yield of the fabricated lot is estimated using modified Poisson yield model [2,3]. Level of contamination is given by the density of defects. For each type of defect, critical area of the layout is used as an estimate of the design's sensitivity to defects [2,4,5,6]. It is also assumed that time required to detect a failure is given by a distribution function with known parameters. It is further assumed that a failure will be considered dominant when the detection count exceeds a certain know threshold value. However, a failure may be caused by more than one type of defect introduced at different steps in the process. One must know in advance which piece of equipment is responsible for the defect. In our model one out of a sub-set of equipment (possibly responsible for the failure) is chosen at random for modification. The failure-defect-equipment mapping is required to model the uncertainty of correct diagnosis. The process modification is assumed to result in a reduction in the density of defects generated by the chosen equipment. The factor of reduction defect density is also assumed to be known.

Yield Learning Simulator - Y4

To examine the above yield simulation methodology, a prototype simulator Y4 (Yield Forecasting) has been implemented in C and tested on a number of examples. The inputs to the simulator are the manufacturing process characteristics (described in previous section), the time horizon for simulation, WIP (number of Lots in Process or Work in Progress) and Screen volume. WIP is supplied so that one can control the number of lots allowed to remain in fabrication line at any given moment. Screen volume is the number of lots to be ignored in the beginning of the simulation so as to allow for the initial transients to settle. The outputs of the simulator are the yield learning curves for each product, the throughput time for each lot, and the total number of lots produced for the simulation time horizon.

Simulation Experiments

To illustrate the application of Y4, we chose two products referred to as A and B, respectively, to be manufactured on a known fabrication line. Product A requires a single poly, double metal process (39 steps) and product B requires a double poly, double metal process (46 steps). Product A is less sensitive to defects than product B. The simulation time horizon was set at 75 weeks and the simulation was repeated for WIP values between 50 and 600 lots in steps of 50.

The experiment was divided into three steps. In the first experiment, we fixed the A:B product mix ratio as 1:1 and compared simulated results with and without failure analysis simulation. In the second experiment, we changed the product mix ratio to 1:2. For the third experiment, we reduced the failure analysis time for only product A by 15%. We used two measures to compare the results of the experiments: *productivity* and *time to 50% yield*. Productivity, in our case, is simply the total number of lots produced during the 75 weeks simulation time horizon. For the second measure, average time required to reach 50% yield is used as measure for effectiveness of yield learning. The results of our experiments are summarized and discussed below.

A. Experiment 1

Figure 2 shows the plot of time to reach 50% yield vs WIP. Figure 3 is a plot of productivity vs WIP. Figure 3 illustrates the fact that learning rate reaches an point for WIP values 300 and 350 for Product A and B, respectively. Beyond these points learning rate decreases because of two reasons. First, failure analysis facility reaches full capacity and second, increasing throughput times causes the improvement to be reflected at a delayed time. On the other hand, productivity reaches its saturation point for WIP greater than 400. Thus depending on the criterion of success WIP values must be chosen accordingly. It is interesting to note that the optimum values for maximum learning rate for Product A and B are not the same. This is because, in our case, product B requires certain equipment not used by product A. This results in less available samples for defects originating in these equipment. Thus raising the WIP level increases the sample size resulting in a more effective failure analysis.

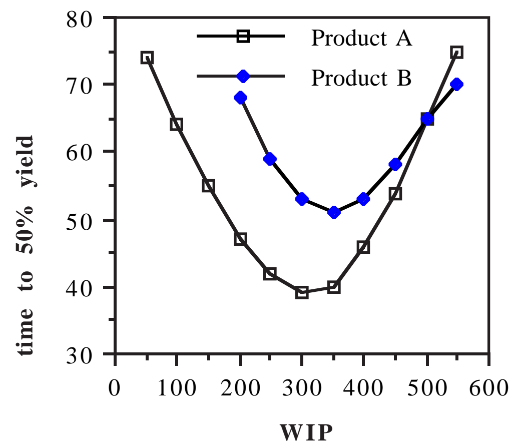

Figure 2. Time to reach 50% yield vs WIP (with failure analysis).

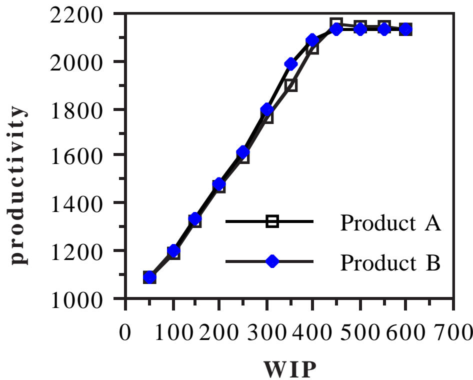

Figure 3. Productivity vs WIP (with failure analysis).

Figure 4 shows the plot of productivity vs WIP for the same fabrication line without the failure analysis simulation. Notice, that the optimum WIP values obtained in the later case is higher than the previous case. This is because, the effect of failure analysis is to increase the equipment downtime and hence the capacity of the fabrication facility is reduced.

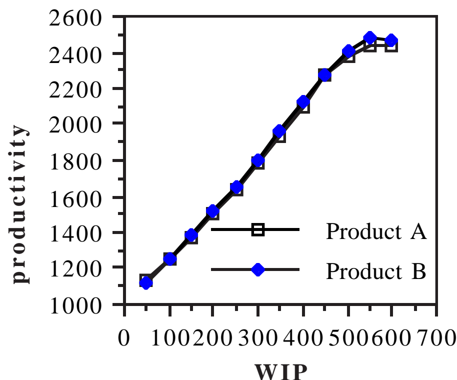

Figure 4. Productivity vs WIP (without failure analysis).

B. Experiment 2

In this experiment we found that there is no gain from the yield learning point of view. But note that twice as much product B is produced thus raising the productivity by 16%. However, productivity of product A is reduced by the same amount. Such manipulation of mix ratio is useful when, for example, product B can be sold at a higher price. By properly adjusting the mix ratio one can maximize the profit.

C. Experiment 3

It can be observed from Figure 5, that the failure analysis times of one product alone can have a profound effect on yield learning rates of the other product in the fabrication line. So, for example, if product A happens to be easier to analyze for failures (like a memory chip), then one can expect a hard to analyze chip like product B to benefit from co-production with product A.

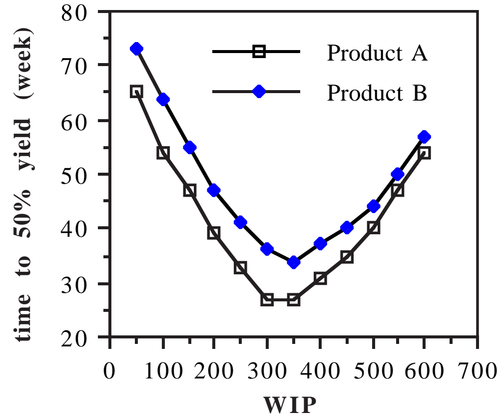

Figure 5. Time to reach 50% yield vs WIP levels (effect of failure analysis).

Summary

In this paper, we have presented yield modeling methodology and its implementation which is suitable for predicting defect related yield versus time curves. The developed tool can be conceivably used to plan resource allocation for optimum equipment utilization, to perform cost analysis and to measure the effectiveness of failure analysis capability. However, the accuracy of the models remains to be verified in an actual manufacturing line.

References

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