AUTOMATED ANALYSIS FOR RAPID DEFECT SOURCING AND YIELD LEARNING

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Abstract

In 1965 when Gordon Moore made his famous observation regarding the exponential growth of semiconductor device capacity, little consideration was given to the fact that the volume of data required to manage the manufacturing process would follow suit. To stay the course predicted by Moore's Law, it will be required that a rapid reduction in process data be achieved through its conversion to useful process control information. This can be partially accomplished through the introduction of new automation technologies that can assimilate manufacturing data from inspection equipment to assist the engineer in the rapid root-cause diagnosis of defect generating mechanisms. These analysis tools will be required to achieve cost-effective yield learning in the next generation fab. In this article, we describe an emerging technology known as Spatial Signature Analysis (SSA) which automates the interpretation of product wafer defect data. SSA is an artificial intelligence method that has been developed in partnership between SEMATECH, Austin, Texas, and the Oak Ridge National Laboratory, Oak Ridge, Tennessee. The method relies on capturing operator experience through a teaching method to emulate the human response to various manufacturing situations. This has been successfully accomplished through the development and application of an image processing-based, fuzzy classifier system. The technique uses data collected from current in-line inspection tools to interpret and rapidly identify characteristic patterns, or "signatures", that are uniquely associated with the manufacturing process. The SSA system then alerts fabrication engineers to probable yield-limiting conditions that require attention. The system has been validated at three major manufacturing sites around the U.S. and is now available as a product through several commercial suppliers. We conclude by discussing future directions required for this and similar technologies if next generation productivity goals are to be achieved.

1. Introduction

Automated analysis of semiconductor wafer defect data has become increasingly important over the past several years as a means of quickly understanding and controlling contamination sources and process faults which impact product yield. Trends towards larger semiconductor wafer formats and smaller critical dimensions have caused an exponential increase in the volume of visual and parametric defect data that must be analyzed and maintained by the semiconductor device manufacturer. This expanse of data has necessitated the development of automation tools for wafer defect analysis [1]. It has been estimated that up to 80% of the yield loss in the production of high-volume, very-large-scale integrated (VLSI) circuits can be attributed to random visual particle and pattern defects [2]. Contamination particles that did not create problems with

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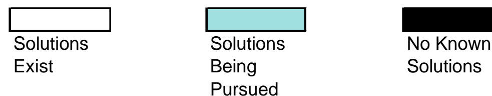
1µm design rules can now be categorized as “killer defects” as critical dimensions dip below 0.25 µm, i.e., defects which result in improper electrical device function.

The need to automate the process of data reduction has been highlighted in the 1997 National Technology Roadmap for Semiconductors as shown in Table 1. This table shows the Technology Requirements information developed by the Defect Reduction Technology Working Group to meet future productivity goals. Under “Fault Isolation Complexity”, it is estimated that complexity in defect sourcing will increase by as much as 170 times over the next 15 years as device density and the number of process steps continue to increase. Data that arises from various product and process inspection points in the fab will become nearly impossible to maintain by purely manual means. This data is generated from in-line inspection tools, in-situ particle monitors (ISPM), pressure sensors, relative humidity sensors, and other fab, tool and wafer monitoring devices located throughput the plant. Coordinating and integrating these data sources is becoming necessary to rapidly control device yield as product complexity increases and fabrication costs continue to rise.

The main issues regarding “Data Analysis for Rapid Sourcing” in Table 1 is the reduction in the time required to source manufacturing problems and recognize trends. It can currently take from weeks to months to manually analyze and bring together all the data sources necessary to make a determination about yield-impacting events in the line. There are many areas of both research and standardization that need to be concurrently pursued if a high degree of automation is to be achieved.

Table 1 – Portion of the Technology Requirements Table for Defect Reduction in the 1997 National Technology Roadmap for Semiconductors.

	1997 *250 nm*	**1999** *180 nm*	**2001** *150 nm*	**2003** *130 nm*	**2006** *100 nm*	**2009** *70 nm*	**2012** *50 nm*
Fault Isolation Complexity							
# transistors in microprocessor (X10^6)	11	21	40	76	200	520	1400
# process steps	350	380	42	450	500	550	600
Fault Iisolation complexity factor (X10^9)	3.8	8	17	34	100	290	640
Defect sourcing complexity trend	1X	2.1X	4.3X	8.9X	26X	74X	170X
Data Analysis fo Rapid Sourcing							
Time Required to Source Problems	days	days	days	hours	hours	hours	hours
Time Required to Recognize Trends	weeks	days	days	hours	hours	hours	hours
Information Sources for Automatic Data Analysis	spatial analysis	time analysis	time analysis	merge	improve	improve	improve
Standardization of Defect Data Output Formats	extend	extend	extend	new	new	new	new
Standard Architecture for Data Transmission / Storage	proprietary arch.	develop standards	adopt	apply	apply	apply	apply
Fuse / Integrate Process and Defect Data from Different Tools	single in-line tools	in/off-line tools	in/off-line tools	extend	extend	extend	extend
Feedback for Automatic Process Control	manual	open loop	open loop	mixture	closed loop	closed loop	closed loop



One such area of automation research that is providing a new means of rapid yield learning is Spatial Signature Analysis (SSA). SSA is an automated procedure that has been developed by researchers at the Oak Ridge National Laboratory to address the issue of intelligent data reduction while providing timely manufacturing feedback [3]. This paper covers the basics of the SSA technology along with progress made to date on factory integration, commercialization, and future research directions.

2. Spatial Signature Analysis

Optical inspection of semiconductor wafers has long been the primary means of investigating the sources of wafer defects. Semiconductor yield engineers use high-resolution images of individual defects collected off-line to assess problems in the manufacturing process. Since high-resolution off-line defect review is time consuming and expensive, process engineers also use low resolution defect wafermaps from in-line optical inspection tools to determine the potential source of problems in the manufacturing process. They accomplish this by analyzing and sourcing unique spatial distributions or "signatures" of defects on the wafer surface. Figure 1 shows an example of a high-resolution optical and scanning electron microscope (SEM) image along with their respective wafermaps containing various spatial signatures. Even when these spatial signatures do not contain significant portions of killer defects (i.e., defects that result in electrical faults), they do provide a diagnostic window into the manufacturing process. SSA attempts to emulate this process to provide the fabrication engineer with faster time-to-results, a critical requirement for effective yield learning and yield management.

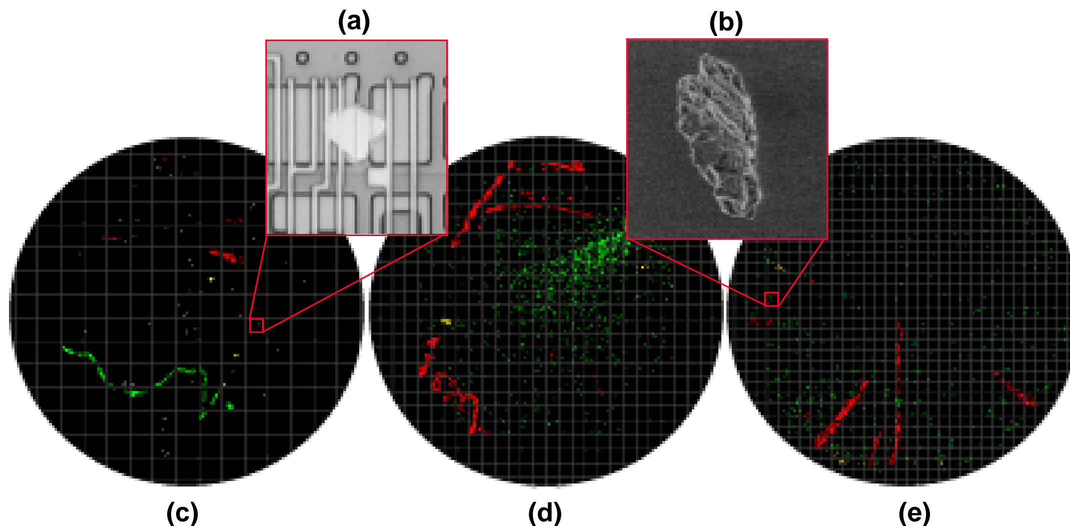


Figure 1 - A spatial signature is defined as a unique distribution of wafer defects originating from a single manufacturing problem. (a) High-resolution optical defect image. (b) High resolution SEM defect image. (c) Single wafer containing scratch signatures. (b) Stack of wafers superimposed highlighting a subtle systematic particle contamination problem. (c) Single wafer showing a spin-coater streak pattern.

SSA attempts to automatically collect defects on a wafermap that come from a single manufacturing source. A user-trained classifier then assigns a label that identifies the root cause. SSA begins the signature classification process by converting the electronic wafermap file into a gray-scale image where each *pixel* is assigned an intensity value according to the number of defects in the subtended area as shown in Fig. 2. Each pixel represents a first level grouping of the individual defects. Connecting pixels according to their proximity to neighbors then forms *clusters* of defects. Clusters of pixels are connected into multi-element *objects* (e.g., a multi-element scratch) by means of a unique advanced clustering procedure. Prior to signature classification, objects are grouped into elemental *sets* depending on their proximity to neighboring clusters and on their morphology [4,5]. These elemental sets are the result of a “divide and conquer” approach to the SSA problem required to reduce the complexity of signature classification. There are four distinct sets in use with the SSA procedure denoted by *global*,

curvilinear, *amorphous*, and *micro-structure*. The assumption is made that every connected or distributed object, i.e., an element of a process signature, can be categorized into one of these elemental sets. These sets are mutually exclusive since an original wafermap defect can only reside in one of the four categories, i.e., there is no overlap.

Each elemental set is characterized individually, i.e., objects belonging to each set have unique descriptive features that relate to the set. For example, elongated objects such as scratches or streaks are assigned to the *curvilinear* set since they have curvilinear attributes such as elongation, compactness, orientation, etc. These objects tend to be associated with mechanical wafer damage. Tightly clustered objects are placed in the *amorphous* set and can generally be associated with problems such as insufficient etching, or other systematic sources which deposit large clusters of defects on the wafer surface that are not related to mechanical damage. Distributed objects such as a ring pattern or a random uniform distribution of particles that are broadly distributed over the wafer surface are grouped into the *global* set. *Global* objects generally consist of sparsely distributed defects and have no highly clustered components yet are treated as one wafermap object since they potentially arise from a single source. *Micro-structure* objects define the final set. These objects are composed of a distribution of pixels whose sub-

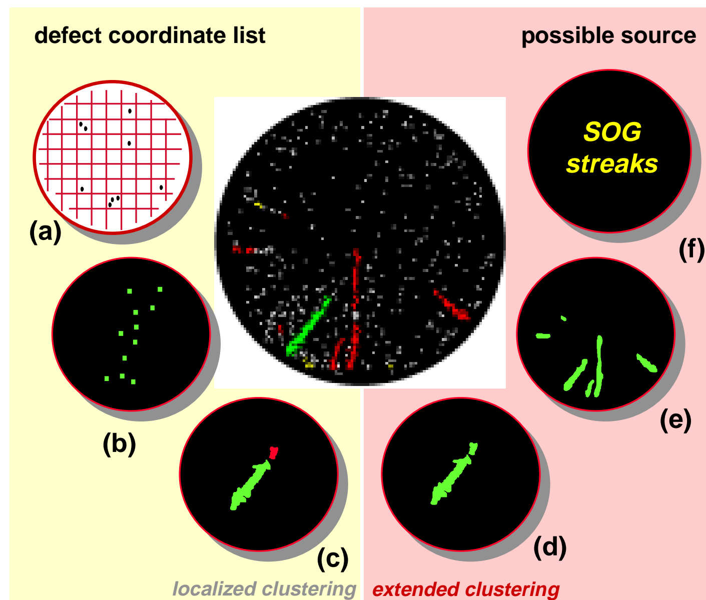


Figure 2 - Schematic representation of the SSA process that starts with a defect coordinate list (a). From the list a grey-scale intensity image composed of pixels is generated (b). Defects are then grouped into clusters (c), objects (d), and signatures (e), prior to classification (f).

pixel defects are organized in a linear fashion. These pixel-level objects arise from planarization processes such as chemical and mechanical polishing (CMP) and are also associated with mechanical damage to the wafer surface but on a micro-scale relative to objects in the curvilinear set.

Figure 3 shows several examples of the variety of signature types that SSA can accurately segment and analyze. Figure 3 (a) shows mechanically induced scratches from robotic handlers, entrained particle streaks from spin-coaters, and double-slot patterns from the improper placement of two wafers in one slot in a wafer boat. SSA also has the ability to analyze reoccurring distribution of defects that do not form discrete cluster patterns such as those just described. Figure 3 (b) shows both random and systematic signatures that arise from particles in process chemicals, gases, and vacuum systems. The SSA classifier can readily separate all of these globally distributed patterns from each other.

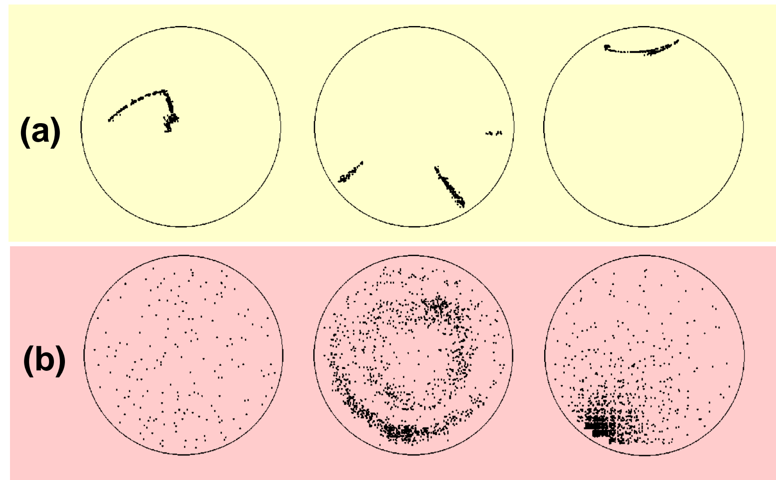


Figure 3 – Various types of signatures found by SSA. (a) Mechanically induced signatures caused by scratching, spinning, and handling, and (b) random and systematic defect distributions caused by tools and processes.

Once an object has been assigned to a high-level set and characterized, its features are sent to a classifier where a user-defined label is assigned to the result. For this work, a pair-wise fuzzy k-Nearest Neighbor (kNN) approach has been adapted [6,7,8] which uses a unique feature reduction procedure to optimize classifier performance [9]. For industrial pattern recognition problems, it has been our experience that non-parametric classifiers such as nearest-mean or kNN [10] apply well. Such classifiers do not require information about the statistical distribution of features. It is difficult to ascertain a statistical parameterization for the large variety of class types encountered. Furthermore, in an industrial setting, it is often required that the classifier system begins to classify new data with few training examples. Bayesian classifiers [11] and neural networks [12] can also work well but generally require large sample populations to estimate the appropriate parameters for their method and would therefore be difficult to implement for this application. This is primarily due to the diverse nature of the patterns that arise for different manufacturing processes and processing facilities coupled with the length of time required to collect large sample populations. Also, over the period of time required to collect large sample sets, acceptable process variations can occur which confuse the boundaries between classes. The pair-wise fuzzy kNN classifier training set can be readily maintained over time (e.g., by including and excluding examples based on time and date), and can operate adequately with relatively few examples for each class [13].

3. Validation of the SSA Approach

SSA research was initiated between SEMATECH and Oak Ridge in 1995. Initial development of the algorithms for signature segmentation and subsequent classification were based on early discussions with fabrication engineers and a broad spectrum of wafermap files donated to Oak Ridge by the various SEMATECH Member Companies. A five month validation exercise was completed in June of 1997 that provided us with the ability to test the maturity of this research and the SSA C++ software library in three different manufacturing environments on three separate products: ASIC, DRAM, and SRAM.

The main goals of the validation exercise are represented in Fig. 4. The SSA method is built upon two primary technologies: *advanced clustering* which segments the defects of a given signature into distinct groups; and *signature classification* which assigns a user-defined class label to each unique grouping. The ability of SSA to accurately source signatures to manufacturing problems, provide new information for statistical process control, provide improved off-line review-tool

Table 2 - Summary of classifier and clustering performance from the three semiconductor manufactures who participated in the validation study.

CLASSIFIER PERFORMANCE	SITE 1	SITE 2	SITE 3
Over all wafers in set	79.10%	72.00%	71.53%
Dominant Signatures	81.36%	79.38%	87.50%
Maps w/ 0-99 Defects	79.11%	61.43%	78.57%
Maps w/ 100-999 Defects	80.49%	73.68%	76.69%
Maps w/ 1000-20,000 Defects	74.32%	76.32%	67.22%

CLUSTERING PERFORMANCE	SITE 1	SITE 2	SITE 3
Over all wafers in set	87.80%	96.57%	82.67%
Dominant Signatures	100.0%	100.0%	100.0%
Maps w/ 0-99 Defects	97.39%	100.0%	100.0%
Maps w/ 100-999 Defects	62.44%	96.61%	94.01%
Maps w/ 1000-20,000 Defects	71.15%	90.48%	75.06%

performance and throughput, and provide new data for yield analysis, all depend on this base functionality. The validation results quantify the performance of SSA for advanced clustering and classification performance.

Table 2 gives a summary of classifier and clustering performance (i.e., segmentation) that were measured at the three manufacturing sites. The first row in the table gives an average classifier performance for all the data analyzed at each site by SSA. This corresponds to 1,933 signatures on 747 wafers that constituted 198 lots and encompassed 50 process steps distributed across the three sites.

The second row of Table 2 shows the summary statistics for all dominant signatures found in the data. A dominant signature is the critical or most relevant signature that resides on the wafer, i.e., the dominant signature reveals the most about the manufacturing process. Note the significance of higher classifier performance for this category of the data. Combined with a clustering performance of 100% for all dominant signatures, this signifies that SSA is very capable of detecting and identifying important wafermap signature events, i.e., those signatures that are most likely to open a window into the manufacturing process and lead to fast process characterization and correction. Also note that this data represents a very broad category of products, processes, and manufacturing culture. When SSA is focused on specific processes, layers, and products, improved classifier performance will be observed.

The remaining rows of performance data in Table 2 show the performance and clustering capability of SSA for various whole-wafer defectivity levels. It was initially anticipated that classification performance would be highest for low-defectivity levels on wafers (due to the simple

morphology of the signature structures) but the data suggests a fairly uniform (at least uncorrelated) distribution of performance across the ranges of 0-99, 100-999, and 1,000-20,000 defects per wafer. Clustering performance, on the other hand, does show a trend towards decreased efficacy as the wafer becomes more populated with defects. This is likely a result of confusion caused by an increasing number of high-density, overlapping signature events.

4. Integration into the Manufacturing Environment

The yield curve shown in Fig. 5 is used to describe how SSA might be applied in the semiconductor fabrication environment. For example, during the *exploratory R&D* phase, there is very low wafer throughput and automation of the analysis is not a high priority. At this stage, SSA would be useful simply as a repository for historical information in the form of the signature library. As the process matures to the *process development* phase, throughput begins to increase and automation becomes an attractive option. In this environment single wafer maps would be analyzed as they are generated by the in-line inspection tools and SSA results would be used to quickly correct process excursions and tool failures.

As the process goes through the *yield learning* phase, wafer throughput will begin to peak. At this point, single wafermap evaluation will still be required to quickly localize mechanical damage and other systematic events such as those that arise during plasma etch or spin-coating. At this point though, wafer stacking will begin to provide insight into the presence of subtle systematic events. As the process matures into the *yield monitoring* phase, there will be relatively few occurrences of mechanical damage. Random defectivity levels will also drop off dramatically as tools and process gases and chemicals become stable and clean. In this environment SSA will primarily view stacks of wafers to keep track of random and subtle systematic distributions of particles over many wafers and/or lots, and to catch the occasional mechanical scratch or other spatially

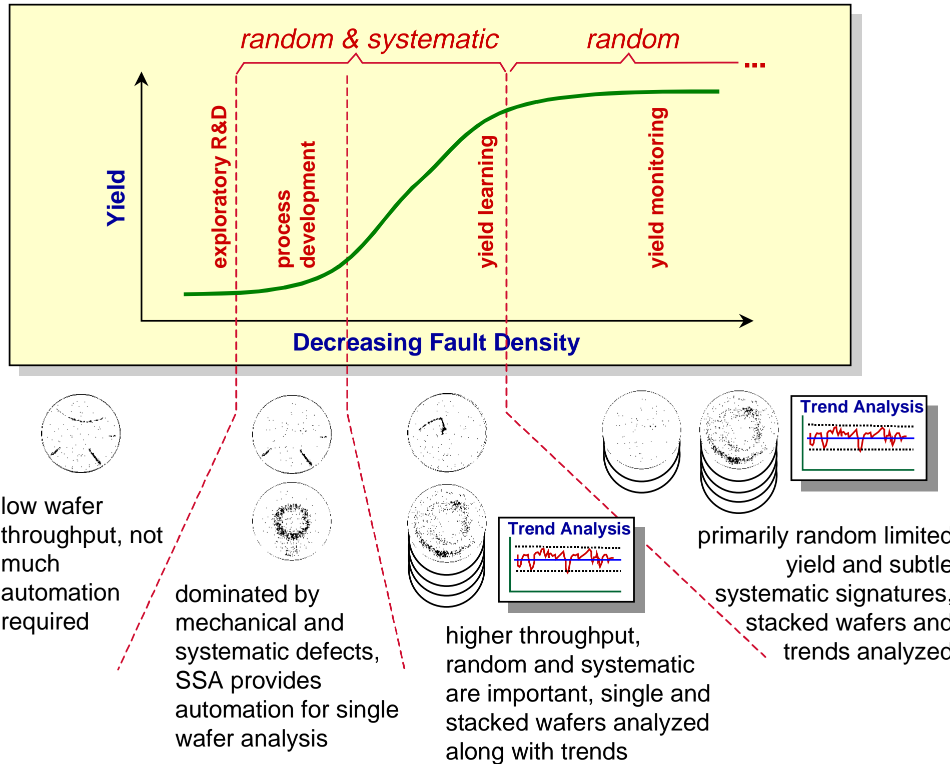


Figure 5 – SSA technology will be applied differently depending on the maturity of the manufacturing process.

localized event that may occur.

Researchers at Oak Ridge have developed a portable C++ library of SSA functions along with an intuitive graphical user interface and a batch-mode interface for automatic wafermap processing. Figure 6 is an example of the software interface showing a signature library and a classified signature result. The current version of the software tool and library is SSA Release 4.0. For licensing information, please contact Nat Olsson at SEMATECH, Austin, Texas, (512) 356-7078.

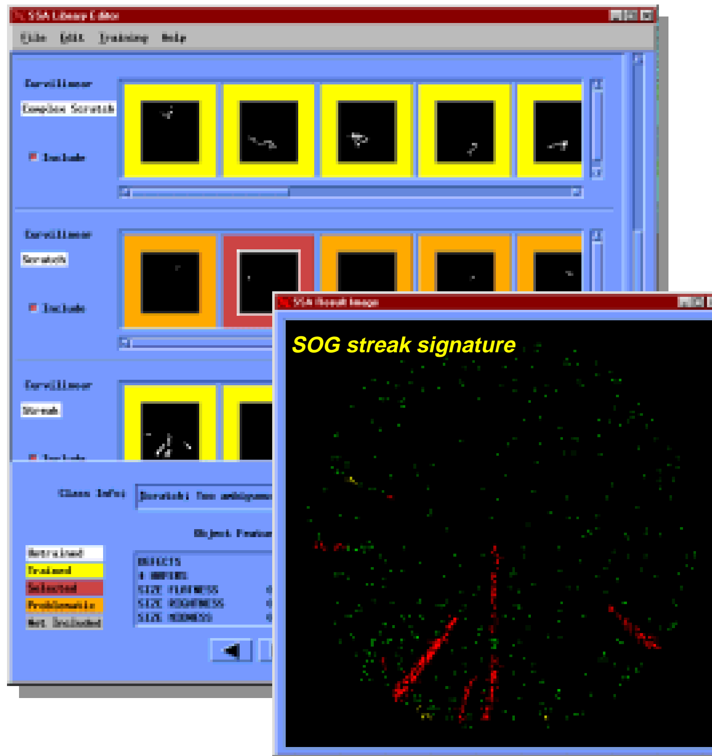


Figure 6 – Example screen showing a signature library and signature result from SSA Release 4.0 software.

There are currently two main pathways through which SSA is finding its way into the manufacturing environment: (1) integration by the manufacturer for use with their internally developed defect data management (DDM) systems, or (2) through licensing of the technology to suppliers of DDM systems and inspection tools. There are currently several licenses of the SSA technology in place for use by the U.S. semiconductor manufacturing industry and the suppliers of defect data management system and inspection tools. The following section describes plans for integration of the technology at Texas Instruments in Dallas, Texas, followed by a discussion of three commercial ventures.

4.1 Integration of SSA at Texas Instruments

Texas Instruments Inc.'s Enhanced Software Defect Analysis (ESDA) system was initially developed in 1990 as a response to data overload while ramping up a new 0.5µm fab. At the time there were no commercially available production-worthy data management systems on the market, and a need was seen to design an in-house system. ESDA was designed to be a yield analysis tool, and is optimized for devices that contain memory. ESDA is a collection of software modules designed to support yield analysis by product and yield enhancement engineers. ESDA gathers all the data available from the fab, i.e., inspection, wafer maps, defect classifications, defect images, bin, bitmap, etc., and stores it in a central location. ESDA performs analysis on

individual data types, e.g., electrical fails and clustering, and integrates different data types for analysis. The most important function of ESDA is in reporting which inspection defects resulted in an electrical failure and which did not [14].

The value of ESDA is gained by allowing the process engineer to access one centralized system to pull together a broad range of data for their particular need. The requested data can easily be gathered into a single succinct report for presentation at daily process problems/shift change meetings. Almost any tool providing measurements of some kind can be connected to ESDA. For instance, in the Dallas Productization 1 Fab, data from the following tools can be analyzed: Ultrapointe, JEOL DRT, Leica review stations, KLA 21XX, Tencor AIT, and Seiko DRT, as well as e-test. Uses of ESDA are seen in Table 3. Turning data into useful information is the strength of a data management system. An overview of ESDA is seen in Fig. 7, with connecting tools noted in generic fashion. All connections are two-way, with the exception of ESDA to the user workstation, which is one way.

Table 3 – Uses of the ESDA system at Texas Instruments

Uses
Loading, creating, and printing wafermaps
Carry-over charts
Linking inspection data to yield
Defect density charts (2D and 3D)
Defect distribution charts
Trend charts
Defect matching
Redundancy analysis

ESDA is fanned out to TI fabs worldwide, including Joint Ventures. Fanout practices allow for fast fab starts and worldwide defect trending. The entire product process is fanned out, i.e., equipment recipes (deposition and etch), inspection/defect detection recipes, defect classification codes, sampling plans, and so on. This practice provides easy comparison of process results and yield, and is accessible worldwide through ESDA. This practice also allows for quick problem solving and recovery when fabs producing the same product can compare notes, especially when something like a particle excursion causes yield loss.

SSA was licensed so that automated spatial analysis techniques could be integrated with ESDA. After a wafer has gone through a defect inspection step, the defect data will go through SSA to remove all the signatures. The reduced data will then be presented to either in-line or off-line automatic defect classification (ADC), where there will be many fewer defects to classify, giving the fab a wafer throughput boost. This combination will provide process signature trends as well as defect type trends. With the addition of signature classifications, the intent is to use SSA to flag problems by wafer or lot that can be tagged by ESDA and sent to automation to put lots on hold. An excellent use of this application will be to detect scratches caused from wafer handling in real time. Long term, the plan is to add e-test and merge SSA and ADC technologies for review tool throughput improvement.

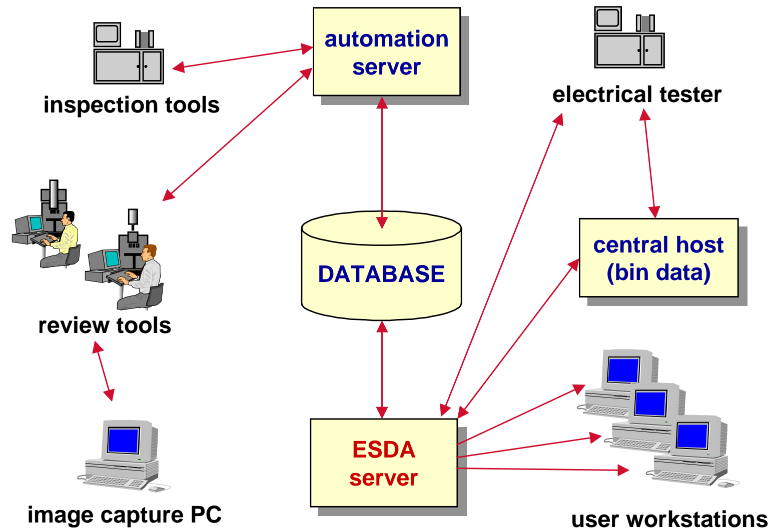


Figure 7 – ESDA system overview.

Training classes are held throughout the year to keep engineers current on any ESDA upgrades, as well as bring new engineers quickly up to speed. ESDA V6.0 is scheduled for release within TI in November 1997, in which SSA will be fully integrated. In the meantime, SSA can be used as a stand-alone tool. There is even an internal ESDA web page for easy access to the latest ESDA release, documentation, patches, and feedback forms.

4.2 Commercialization of SSA

As mentioned above, there are currently several licenses in place for the SSA technology. Semiconductor equipment suppliers who manufacture data management systems and inspection tools have licensed the technology as a means of providing data analysis automation. These companies have initially considered using SSA to add capabilities to their data management systems but the technology may eventually find application as an integral component of in-line inspection tools. The "best" way to integrate SSA technology is yet to be determined. But it will likely fit into several application areas. Possibilities include advanced clustering and signature classification on in-line inspection tools, automated data analysis at the data management system level (for reporting, alarming, SPC, etc.) and intelligent sampling and analysis to improve throughput and performance of off-line automatic defect classification (ADC) for optical and SEM review tools. As an indication of the commercial viability of the approach, the following companies are developing or have already announced new SSA-based products for use in the data management environment.

Defect & Yield Management (DYM), Inc. of Bedford, Massachusetts believes the success of many semiconductor products has become increasingly dependent on how quickly and how accurately individual processes can be analyzed and controlled. DYM provides integrated defect analysis systems that encompass equipment interface, database, and graphical user interface. DYM has plans to integrate SSA technology with the Quest™ data management system currently distributed by KLA-Tencor, Inc. They will be announcing a product during the 4th quarter of 1997. SSA will be complementary to their NEDA™ product (NeuralNet™™ Engineering Data Analysis) that intelligently recognizes wafer bin map patterns from probe bin data using a neural network classifier method. For further information please contact Gary Green (617) 271-0120.

Knights Technology, Inc., of Sunnyvale, California, is a software company serving the process manufacturing and electronic design market. Their client-server yield enhancement software helps their customers with rapid yield learning, low yield analysis, wafer inspection, defect reduction and

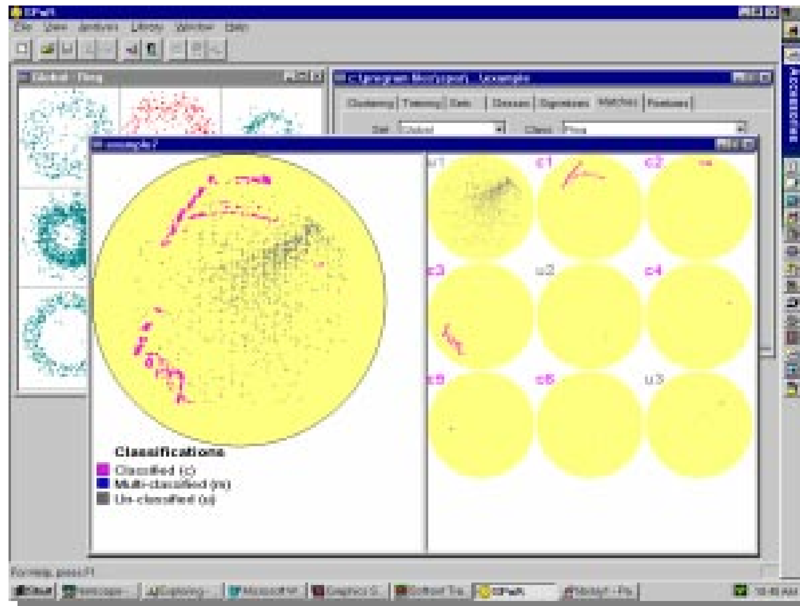


Figure 8 – Software interface to Knights Technology's new SPaR™ product for spatial signature analysis.

high yield maintenance. Knights has announced the availability of a new spatial analysis product called SPaR™ which is based on the SSA technology. The interface for the system is shown in Fig. 8. Future releases of the product will include direct access to their Yield Manager™ client-server software system, alarm capabilities for SPC, automatic signature library generation, and other features to improve performance and ease of use. For further information please contact Mr. David Guidry at (408) 988-0600.

LPA Software, Inc. of Burlington, Vermont, established the Semiconductor Solutions Division to provide products, custom development and system integration services for semiconductor factory automation worldwide. Their DefectEvaluatior System™ (DES) is known for its ability to quickly and reliably manage large amounts of defect data coming from multiple detection sources. LPA will include pattern recognition capabilities in their products beginning 4th quarter of 1997. Advanced capabilities will be based on SSA technology. These capabilities will be integrated into their DES and DefectAnalyzer™ systems. LPA also offers SSA Release 4.0 distribution, installation, maintenance, and training. For further information please contact Mr. Carl R. Hoffman at (802) 862-2020 x260.

5. Future Research and Development

SSA represents a new approach to automated and rapid data reduction in the fab. The data sources being considered for SSA are currently optical in-line wafermap and electrical test data. This represents a "product" view of the process as shown in Fig. 9. An integration of both product and process data in an automated analysis environment has the potential to provide the industry with yield management capabilities well beyond current means. Results such as improved wafer throughput in the fab, rapid root cause determination, higher resolution SPC, real-time yield analysis, and automated tool control are all possible. Current efforts related to this research have focused on in-line tool data such as optical microscopy, laser scattering, and electrical binmap

and sort data. New efforts to incorporate off-line data sources for ADC and to investigate trend recognition in SSA data are proposed as a next step.

It has been proposed that SSA be extended to work with off-line defect review and ADC using SEM. This will be a high priority issue as device geometry dips below the optical defect detection limit at 180 nm in the year 1999. Note that the minimum critical defect size will be at roughly one-half the critical dimension or 90 nm, i.e., below the detection limit of current optical inspection technology. Technologies such as SSA will be required to assist in maintaining realistic wafer throughput through inspection tools as SEM technology moves from an off-line review and CD measurement tool to an in-line inspection tool somewhere between the year 2000 and 2006.

Over time, SSA will not be sufficient to address these automation needs. Advances must be made in temporal signature analysis as well, i.e., trend analysis in the wafer and lot data. SSA provides a higher resolution of event categories (e.g., scratches, streaks, random defect densities, systematic distributions, etc.) which should assist the manufacturer in performing statistical process control (SPC). SPC control charts assist the manufacturer when a process is beginning to drift out of specification but are currently limited to considering only gross particle or simple cluster counts. Trend analysis can take this concept further by looking for patterns in the time-dependent results of SSA. These patterns would be representative of temporal signatures

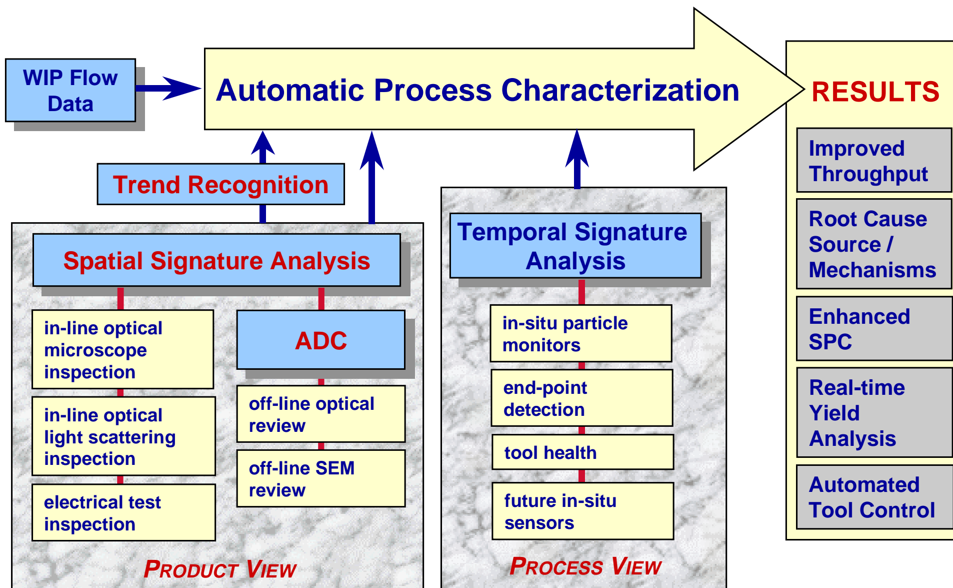


Figure 9 – Conceptual data flow showing a process and product view of the data abnalaysis. SSA currenlty analyzes product data from in-line inspection tools.

that could reveal subtle information about a process that are still within SPC control limits but which can be indicative of impending excursions. One example application of trend analysis would be for improved predictive maintenance.

Temporal analysis will include time based sensors (ISPM, temperature, pressure, RF, etc.) as well as trend analysis based on SSA and will require an integration of these data sources from various points in the process to achieve a truly automated understanding of product yield issues. The ability to integrate off-line inspection tool data (e.g., SEM, EDS, Auger, ToF SIMS, X-ray, TEM, etc.) into a “rapid sourcing” analysis environment will also be necessary to understand the elemental composition of various contamination sources and their deposition mechanisms. Needless to say, the architecture for this technology is in its infancy and requires continued support on an industry-wide level if future productivity goals are to be achieved.

Enhanced yield prediction and analysis also represents another area for application of SSA technology. Yield is defined as *the fraction of total input transformed into shippable output*. Yield can be further subdivided into categories such as *line yield*, *die yield*, and *final test yield* [15]. As the signature and process information generated by SSA becomes more accepted as a reliable representation of the current and historical state of the manufacturing process, it will provide new opportunitites to investigate and predict yield. Current yield models are best suited to mature processes and do not accommodate systematic defect distributions in an optimal way. They rely on spatial approximations that are only roughly correct [16, 17]. These approximations are generally required to break with the fundamental tenets of Poisson-based yield modeling e.g., that the distributions of yield-limiting events are sparse and uncorrelated [18]. Having the new statistics provided by SSA should motivate new model activities. For example, while most yield predictors rely heavily on active device area, random defectivity measurements, and wafer zone approximations, SSA data can provide an accurate representation of the various random and clustered systematic events. Coupled with electrical test information, these various defect signature categories can be characterized according to their ability to impact device yield. While this data is available to the manufacturer today, the tedious job of gathering and maintaining statistically relevant samples over an extended period of time is untenable and yield models that use this resolution of manufacturing detail have not yet been developed.

6. Conclusion

Automation tools to rapidly source defect mechanisms to their root cause are becoming more necessary as semiconductor product and process complexity continues to increase. SSA and related concepts of automated data analysis have been demonstrated to be a viable approach for staying on Moore's productivity curve but this is only a beginning. Temporal analysis, which results in the recognition of signatures in spatial trend data, ISPM data, and other tool health sensors will be required over time to achieve a more complete level of data integration and to achieve a higher rate of yield learning and yield control. It is anticipated that industry support of SSA and other related analysis techniques, will ultimately result in the achievement of many of the goals put forth in the 1997 National Technology Roadmap for Semiconductors.

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8. Biographies

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He has been performing research with the semiconductor industry since 1991, performing R&D for optical image defect classification and electronic wafermap spatial signature analysis and data reduction. Dr. Tobin is a member of the Optical Society of America and the International Society for Optical Engineering (SPIE) where he is currently serving as a co-chairman for the SPIE Conference on Machine Vision Applications in Industrial Inspection. He is currently a member of the Defect Reduction Technology Working Group for the Semiconductor Industry Association National Technology Roadmap for Semiconductors. Dr. Tobin has a Ph.D. in Nuclear Engineering from the University of Virginia, Charlottesville, Virginia, and an MS in Nuclear Engineering and BS in Physics from Virginia Tech, Blacksburg, Virginia.

SHAUN S. GLEASON is a research and development staff member with the Image Science & Machine Vision Group at the Oak Ridge National Laboratory (ORNL), Oak Ridge, Tennessee. He researches algorithm development and has authored and co-authored 21 publications in the areas of image processing, feature extraction and analysis, and pattern recognition. He was the principal investigator of a highly successful optical automatic defect classification (ADC) cooperative research program with KLA Instruments Corp. that ended in 1994 and resulted in an ORNL Significant Event award and the filing of a patent with the U.S. Patent Office. Since 1991, Mr. Gleason has worked in the area of automated semiconductor defect inspection with SEMATECH in the areas of ADC and SSA. Mr. Gleason has a BSEE and MSEE from the University of Tennessee in Knoxville and is currently a Ph.D. candidate.

FRED LAKHANI is a project manager within the Contamination Free Manufacturing organization at SEMATECH, Austin, Texas. He is currently managing programs on Spatial Signature Analysis, SEM-based ADC, and Semiconductor Yield Modeling. Prior to joining SEMATECH, Mr. Lakhani has held a variety of positions in device engineering and yield management. He has published numerous technical articles in his field. Mr. Lakhani has a BSEE from the University of Texas at Arlington, an MSEE in Materials and Devices from the Southern Methodist University and he is a recent graduate of the Institute of Managerial Leadership at the University of Texas at Austin.

MARYLYN H. BENNETT has been a member of the technical staff at Texas Instruments, Inc. for sixteen years. Ms. Bennett spent two years as a TI assignee to SEMATECH, where she became the project manager for Defect Detection and Analysis, working on automatic defect classification and advanced patterned wafer inspection. She returned to TI in January of 1996, and continues working as the TI champion for automatic defect classification. Ms. Bennett is a member of SPIE, the Microscopy Society of America, and the Electrochemical Society for which she serves as treasurer of the Electronics Division and member of the Finance Committee. Ms. Bennett is the author and co-author of thirty-five technical publications.

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